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UNITED STATES PATENT APPLICATION

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for

INTEGRATED CIRCUIT

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BACKGROUND OF THE INVENTION

The present invention relates to the field of integrated circuits, and in particular to integrated circuits that include at least two circuit components that are formed on a common semiconductor substrate and which each have self-contained supply voltage systems.

Integrated circuits may include at least two circuit components that are formed on a common semiconductor substrate and which each have self-contained supply voltage systems. In addition, each of the two circuit component may include self-contained bonding spots for receiving an externally supplied voltage. Separate supply voltage systems of this type may be necessary to meet EMC requirements. In conventional technologies for highly integrated circuits, the semiconductor substrate is p-conductive and is connected to the power supply nodes of the two circuit components that carry the lowest voltage potential "Vss" among the applied potentials, such that the Vss potentials of the two circuit components are coupled by one substrate resistance.

One or more connections in the form of signal lines are often present between the two circuit components. The desirable isolation of the supply voltage systems for the individual circuit components may lead to problems in the event of excessive voltages (EOS, electrical overstress). This is particularly true in the event of electrostatic discharge (ESD), since the supply voltage systems of the individual circuit components occupy a relatively smaller area and supply a smaller number of components than does a corresponding system comprising the entire integrated circuit. Therefore, such supply voltage systems react with greater sensitivity to the switching operations of individual components, and differential voltages are transferred from one

circuit component to another through the signal lines and are thus able to reach sensitive circuit components, such as the gate-oxide layers, which may be destroyed by these voltages.

A prior art technique includes coupling the supply voltage systems for multiple circuit components integrated on a common semiconductor substrate using coupling circuits, as shown in FIG. 1. FIG. 1 is a schematic illustration of a prior art integrated circuit 100 that includes first and second circuit components 1, 2, respectively. The first and second circuit components 1, 2 receive supply potentials Vcc1, Vss1, or Vcc2, Vss2, as shown through bonding spots 5. Under normal operating conditions Vcc1 = Vcc2, and Vss1 = Vss2. The integrated circuit 100 also includes first and second coupling circuits 3, 4. The first coupling circuit 3 receives Vcc1 and Vcc2 on lines 102, 103 respectively, while the second coupling circuit 4 receives Vss1 and Vss2 on lines 104, 105 respectively. Each coupling circuit includes antiparallel connections of two PNP transistors 6. Whenever excess voltage mutually disturbs the supply voltage systems of the first and second circuit components 1, 2, the transistors 6 produce a compensation of voltage, such that a portion of the current flows from the emitter to the base, while the rest continues to flow to the collector.

The PNP transistors 6 each have the semiconductor substrate as the collector, an n-doped well formed in the substrate as the base, and a p^+ region inside the well as the emitter. The effect of this arrangement is that when one of the coupling circuits 3, 4 opens in response to an excessive voltage of one of the transistors 6, although part of the compensation current (from the emitter to the base) will flow from one supply voltage system into the other, another part nevertheless will unavoidably flow directly from the emitter into the substrate representing the collector.

A problem with these conventional coupling circuits is the considerable area they utilize on the substrate. Considerable area is required because each of the coupling circuits, one of which is required for each supply voltage to be compensated, has two transistors 6. An addition considerable area is required is because essentially holes are involved in the current flow through the transistors 6. The mobility of holes is less than that of electrons, and therefore require comparatively greater coverage areas of the doping zones in order to achieve a volume resistivity of the transistors that is sufficiently low for effective coupling.

Therefore, there is a need for an integrated circuit that includes at least two circuit components and separate supply voltage systems for the different circuit components, which integrated circuit has coupling circuit that has a small surface area requirement between the supply voltage systems.

SUMMARY OF THE INVENTION

A base of the transistor is preferably formed by the substrate itself, or, more precisely, by a region of the substrate contiguous with collector doping zones and emitter doping zones of the transistor, and the resistance between the base and the potentials of the two systems coupled by the coupling circuit is the intrinsic resistance of the substrate between its region forming the base and one of each contact doping zone that is conductively connected to the collector or emitter through a metallization applied to the substrate. To obtain an identical coupling behavior for the transistor in both directions, the collector and emitter of the transistor are preferably symmetrical, such that the arrangement may also be termed a transistor with a double emitter.

The coupling circuit may be implemented with a single transistor, the dimensions of which are fixed by the desired volume resistivity. Greater flexibility of design with respect to

accommodating the coupling circuit on one substrate surface without an increased area requirement is provided by employing multiple transistors. These may as a rule be distributed independently of each other on the substrate surface.

A space-saving design results by creating the transistors using a plurality of doping zones of the second conductivity type, which are alternately connected to the first or second of the two power supply potentials. Specifically, if a doping zone connected to the power supply potential of the first circuit component is surrounded on both sides – in each case with an intermediate base zone having the natural doping of the substrate – by doping zones connected to the power supply potential of the second circuit component, then the resulting arrangement is the equivalent of two parallel transistors. In an arrangement of this type, the surface area requirement for two transistors is significantly less than the double-sized space requirement needed for two individual transistors. This savings in space may be increased even further if more than two transistors are created by providing an alternating arrangement of doping zones connected to the two power supply potentials.

To ensure the same behavior of these transistors, the transistor doping zones should be appropriately arranged in series in an equidistant configuration. The contact doping zones are preferably located at the ends of the series. In one embodiment two contact doping zones are sufficient for a plurality of transistors.

In the case of this type of series arrangement of contact doping zones and emitter-forming doping zones, preferably each emitter-forming doping zone directly adjacent to a contact doping zone is metallically conductively connected to this contact doping zone. In the event of an excess voltage, this arrangement reduces the risk of a breakdown between a contact doping zone

connected to the first circuit component and a emitter-forming doping zone connected to the second circuit component.

To achieve identical coupling behavior in both directions, the number of emitter-forming doping zones of the second conductivity type is an even number for the symmetry for the coupling circuit. In one embodiment the number of doping zones may be four – which corresponds to a parallel circuit of three transistors.

To avoid the undesirable interaction between the transistors of the coupling circuit and the circuit components, at least one transistor of the coupling circuit may be surrounded by a shielding doping zone of the second conductivity type. A shielding doping zone of this type is biased in the nonconducting direction, such that a barrier layer is formed between this zone and the substrate.

The shielding doping zone preferably runs in an annular pattern along the surface of the substrate. It thus does not prevent every current flow from the at least one transistor of the coupling circuit through the substrate to the circuit component, but rather forces the charge carrier to follow an alternate route into the depth of the substrate. This increases the route length, and thus the effective resistance of the substrate, between the transistors of the coupling circuit and the circuit components. The contact doping zones of the coupling circuit are preferably surrounded by the shielding doping zone.

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic illustration of a prior art integrated circuit;

FIG. 2 is a schematic illustration of a coupling circuit;

FIG. 3 is a plot of the current-voltage characteristic of the coupling circuit illustrated in FIG. 2;

FIG. 4 shows an example having the surface structure of a coupling circuit according to an aspect present invention;

FIG. 5 is an equivalent circuit diagram of the surface structure in FIG. 4;

FIG. 6 shows a modification of the surface structure of FIG. 4;

FIG. 7 shows a further modification of the surface structure in FIG. 6;

FIG. 8 is a cross-section through the structure of FIG. 7 of the surface structure in FIG. 6;

FIG. 9 shows a further modification of the surface structure.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 is a schematic illustration of a coupling circuit 200, which may be utilized as a replacement to the coupling circuit illustrated in FIG. 1. The coupling circuit 200 includes an NPN transistor 11, the geometry and doping of which are symmetrical. The transistor 11 includes a first emitter 202 that is connected on a line 204 to first voltage potential Vss1, and a second emitter 206 that is connected on a line 208 to second voltage potential Vss2. The two power supply potentials Vss1, Vss2 are each connected through identical resistances 12 to transistor base 210.

FIG. 3 is a plot 300 of the current-voltage characteristic of the coupling circuit illustrated in FIG. 2. Current is plotted along vertical axis 302 and voltage is plotted along horizontal axis

304. In response to small differences between the two power supply potentials, the behavior is resistive and is determined by the resistances 12 (FIG. 2). The activity of the transistor 11 is activated in response to increasing voltages, and the compensating current I flowing through the coupling circuit 200 increases with voltage V at a greater than linear rate.

FIG. 4 illustrates a first example of a coupling circuit 400. The coupling circuit 400 includes a plurality of doping zones 14-19 formed adjacently in a series on a p^--doped semiconductor substrate. The most external of these zones are p^+-doped and designated as the contact doping zones 14, 19. The intermediate zones, that is the emitter doping zones 15-18, are n^+-doped. Surface metallizations of the doping zones 14, 16, 18 are connected to first voltage potential Vss1, while those of the doping zones 15, 17, 19 are connected to the second voltage potential Vss2. Surface strips 20, 21, 22 of substrate 13 are located between the emitter doping zones 15-18, and have the original p^--doping of the substrate in a doping concentration unaltered by the generation of doping zones 14-19. The surface strips 20, 21, or 22 each function as the base of a symmetrical transistor, the two emitters of which are formed by the two emitter doping zones contiguous with the relevant surface strips 20. In the event of a voltage difference between Vss1 and Vss2, the contact doping zones 14, 19 allow a flow of current through the substrate 13 from one contact doping zone 14, 19 to another. This current flow determines the corresponding electrical potentials effective in the region of individual surface strips 20-22. The equivalent circuit diagram shown in FIG. 5 thus corresponds to the layout of FIG. 4. The two middle emitter doping zones 16, 17 of the layout of FIG. 4 correspond to the two symmetrical npn transistors T1, T2, or T2, T3, the bases of which are each formed by surface strips 20, 21, 22. The resistances R between contact doping zone 14, the bases of the transistors, and contact doping zone 19 result from the low intrinsic conductivity of the weakly doped substrate 13.

FIG. 6 shows another design for a layout of a coupling circuit. The design differs from the layout of FIG. 4 in that the emitter zones connected to Vss1 or Vss2 are transposed such that the respective adjacent doping zones 14 and 15, or 18 and 19, are connected in parallel through a metallization. The fact that this approach increases the distance, compared to the layout of FIG. 4, between the contact implantation zones 14 or 19 and the immediately adjacent emitter doping zones 16, 17 connected to the other power supply voltage – thereby also increasing the substrate resistance by a corresponding amount – reduces the risk that an excess voltage pulse will cause a breakdown at the pn boundary of the emitter doping zones. That is, the dielectric strength is enhanced, as compared with the layout of FIG. 4, with the same dimensioning and arrangement of the doping zones; or the width of the surface strips between contact doping zones 14, 19 and adjacent emitter doping zones 15 or 18 may be reduced with the dielectric strength remaining the same, thereby further decreasing the space requirement of the coupling circuit.

FIG. 7 shows a further modification of the layout design of FIG. 6. Since the transistors formed by surface strips 20-22 and the adjacent emitter doping zones 15-18 are connected to substrate 13, a shielding doping zone 23 is provided to reduce the interactions between the transistors of the coupling circuit and the elements of circuit components 1, 2. The shielding doping zone is formed by n-doping with a high penetration depth into the substrate 13. On the surface of the substrate 13, the shielding doping zone 23 is highly n-doped on a small cross-sectional area so as to form a contact zone 25, which is in conductive contact with a metallization 24 deposited on the substrate surface. The shielding doping zone has low n-doping over the majority of its cross-section, as indicated by the widely spaced hatching, and a lower doping concentration than in the other n-doped emitter doping zones. As the cross-section in FIG. 8 shows, the shielding doping zone 23 significantly lengthens the current path from the emitter

doping zones 15-18 to the adjacent elements of the circuit components 1 or 2 (not shown in FIG. 7). The effect of the shielding is due here to a positive potential applied to the shielding doping zone 23 over the metallization area 24, which potential results in the formation of a barrier layer at the pn junction between the shielding doping zone 23 and the substrate 13.

FIG. 9 shows another modified design for the layout of FIG. 6. The shielding doping zone 23 is configured in an annular shape which surrounds emitter doping zone 15-18. In contrast to the design of FIG. 7, the contact zone 25 is not arranged in an annular configuration around the transistors of the coupling circuit but is limited to two islands, each of which is conductively connected to one of the two potentials Vss1, Vss2.

Since it is possible to keep the doping concentration low in shielding doping zone 23, its conductivity may be maintained at a low value similar to that of the substrate 13.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: